A 0.5-12 GHz HYBRID MATRIX DISTRIBUTED AMPLIFIER USING COMMERCIALLY AVAILABLE FETs

S. D'Agostino, G. D'Inzeo, G. Grifoni, P. Marietti and G. Panariello.

University of Rome "La Sapienza", Department of Electronics
Via Eudossiana 18, 00184 Rome ITALY.

Abstract

In this work we present a matrix distributed amplifier for a coherent high bit-rate optical receiver front-end. A gain of 20 dB in the 0.5-12 GHz with a noise figure between 5-8 dB over the whole frequency range has been obtained together with a low VSWR as the experimental results prove. The layout is very simple in comparison to other hybrid realizations reported in literature and is fully related with the lumped elements of the circuit schematic. The computed results obtained using a small signal model for each FET fit rather well with measurements.

Introduction

The matrix amplifier (Fig. 1) has been presented in 1987 by Niclas and Pereira [1]. This circuit allows a high gain per unit area and low input and output VSWR with respect to a usual equivalent two stage distributed amplifier. Since it occupies less chip area, particularly in monolithic form [2-3], the related cost is considerably lower.

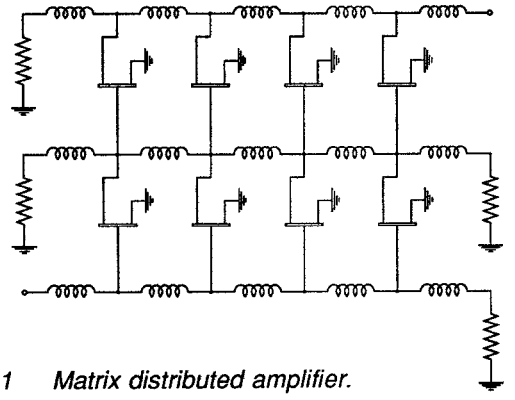
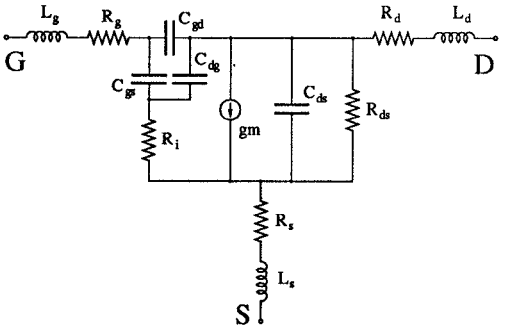


Fig. 1 Matrix distributed amplifier.

Among the many advantages with respect to a usual equivalent two stage distributed amplifier, that will be discussed later on, the two-tier amplifier shows a significantly better noise behaviour [4].

In this work we describe the design and experimental results of a 2x4 hybrid amplifier module. This circuit utilizes eight commercial HEMT (*NEC* NE20200). In Fig. 2 the HEMT small signal equivalent circuit obtained with a minimum noise performance biasing is shown.



L_g = 0.1 nH	gm = 45 mS
R_g = 2 Ω	τ = 2.5 ps
C_{gs} = 0.20 pF	G_{ds} = 5 mS
C_{gd} = 0.016 pF	C_{ds} = 7.2 fF
C_{dg} = 6.7 fF	R_d = 4 Ω
R_S = 3.5 Ω	L_d = 0.13 nH
L_S = 0.02 nH	R_i = 4 Ω

Fig. 2 Equivalent circuit of NE20200 (NEC).

The amplifier, realized in hybrid technology, incorporates a novel scheme which allows to bias a single stage of the two tiers amplifier (two rows of active devices) with a unique controlling resistance and, at the same time, to cascade the two FETs of each stage.

Design consideration

The microstrip pattern is realized on alumina substrate; use of such a material is justified by its well experimented technology, which allows the product to be much more reliable than those employing different materials (as quartz or RT duroid). We have chosen a 508 μm-thick substrate which shows a rather good resistance to mechanical stress and allows an easier design for higher frequency operation.

The choice of the biasing circuit has been one of the critical problems tackled during the design. We have adopted a self-biasing arrangement, as shown in Fig. 3. Such a solution allows biasing of all active devices by making use of two dc voltage (V_g=-0.55 V and V_d=4.55 V) and no power dissipation in the termination resistors. The microstrip line linking the gates of the first-tier FETs is connected to V_g, which gives the proper gate-source voltage.

CH2870-4/91/0000-0289$01.00 © 1991 IEEE

The connection is made by bond-soldering on the upper plate of the capacitor placed externally to the alumina chip after the termination resistor. Current doesn't flow on the gate-line so that there is no potential drop through the resistor.

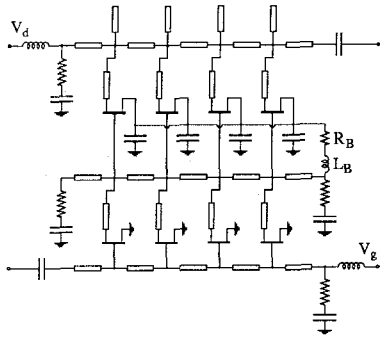


Fig. 3 Schematic of the matrix amplifier with biasing circuit.

The V_d voltage is connected to the microstrip line linking the drains of second-tier FETs. It provides the drain-source voltage of all FETs and the gate-source voltage of the second-tier FETs powering the units through the upper side of the capacitor located on the 50 Ω RF-output line. We want to point out that it is not possible to adopt a solution similar to that used with V_g. As a matter of fact, using the external capacitor situated after the upper termination resistor allows flowing of all drain currents, totaling 40 mA, through the latter and causes excessive power dissipation.

To justify the biasing scheme of the amplifier, let us consider the circuit of Fig. 4: at signal frequencies inductor L_B provides isolation between the source of FET_2 and the drain of FET_1, in such a way that the two FETs result cascaded; in addition, capacitance C_B grounds the source of FET_2. The two FETs are dc connected also by the series L_B-R_B and the voltage through R_B sets the V_{gs} of FET_2, at the same value as that of FET_1, as since the two FETs have the same drain current I_D, V_d divides in two, allowing all active devices to operate in similar bias conditions.

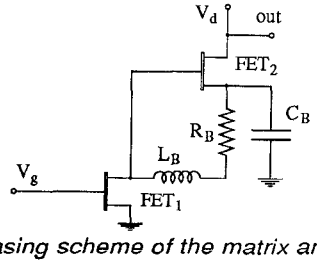


Fig. 4 Biasing scheme of the matrix amplifier.

Since parameters of commercial available FETs show variability of the order of 10 % from the typical values, resistor R_B is tunable over three different values to better adjust biasing of active devices.

The novel biasing solution adopted for second-tier FETs' sources is noteworthy: insertion of capacitors between FETs allows RF grounding, maintaining all sources at the same dc voltage; in such a way cumbersome connection lines are avoided.

The circuit was Touchstone™ simulated and optimized with respect to component values.

In a practical hybrid amplifier, an important limitation to the increase of the bandwidth derives from the difficulty of reducing the inductor length in the input line below a minimum value. The signal travelling along the input line undergoes an attenuation which increases with the distance between the gates of first-tier FETs; a limit to high frequency performance is then given by the gate line attenuation [5]:

$$A_g = \mathrm{Re}\left\{\cosh^{-1}\left[1 + \frac{j\omega L}{2\left(R_i + \frac{1}{j\omega C_{gs}}\right)}\right]\right\}$$

where L is the inductance between the gates and R_i and C_{gs} are parameters of the FET equivalent circuit.

The minimum value of the distance between two adjacent gates results essentially from two technological needs: the active devices chip size and the spacing necessary for source-to-ground bonding, as the insertion of the bonding machine's tip (Fig. 5) between contiguous first-tier FETs has to be allowed.

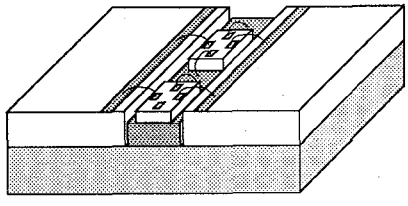


Fig. 5 Side-section of the chip showing "not shaped" carrier.

This problem has been solved by shaping the carrier so as to allow the bonding near FETs front rather than near their sides (Fig. 6) as normally used. Such a solution permits a decrease in the minimum possible distance between first-tier FETs: this has been fixed at 400 μm. During optimization we have then set the length of the lines linking the gates to 800 μm.

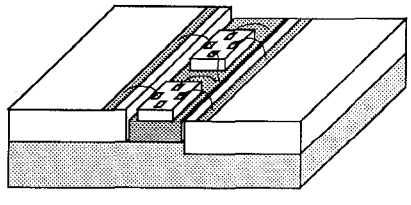


Fig. 6 Side-section of the chip showing "shaped" carrier.

Referring to the second tier FETs, a similar gate line length cannot be assumed because of the insertion of capacitors between the active devices; then, we have included in the optimization routine drain and gate linking-line elements of the upper FET row. Such a process led us to the above mentioned circuit, which is characterized by gate and drain line whose length become shorter the closer the element is located towards the output terminal of the gain module, in accordance with what was demonstrated to be a better solution in order to minimize the reverse amplification and to obtain a flat gain in a simple distributed amplifier ("declining drain line length") [6].

The alumina chip obtained by the photolitographic-etch-resistor stabilization processes had to be subdivided into three individual sections. To avoid cracking of the chip during the sawing process, we let the distance between the two FETs rows at a minimum of 1600 μm. The layout of the matrix amplifier is shown in Fig. 7.

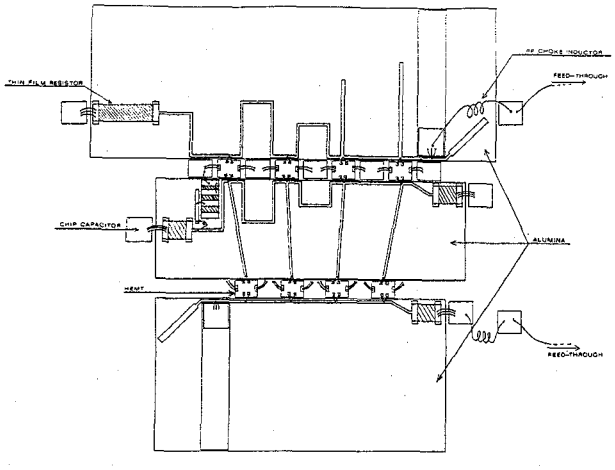


Fig. 7 The layout of the matrix amplifier.

The overall chip dimensions are 6.8x7.8 mm; the microstrips' width linking each FET is about 40 mm.

Fabrication

The three section of alumina have been assembled on a 900 μm-thick gold plated kovar carrier to give a single module. The thickness chosen, nearly twice the substrate thickness, prevents carrier warping and consequent cracking of alumina and at the same time creates a very direct ground at high frequencies.

On the shaped carrier, two small ground ribs, made of gold plated copper, are brazed between the adjacent alumina chips. The ribs are high enough to bring the gate of the FETs at the same level as the microstrip gate lines, in order to obtain minimum gate bonding lengths (Fig. 8); on the other hand, drain bonding resulted longer than that of the gates.

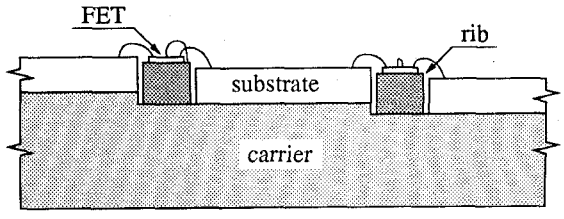


Fig. 8 Side-section of the chip.

To reduce parasitics, seven bondings have been employed to connect the microstrip to the external capacitors. Fig. 9 presents a photograph of the module.

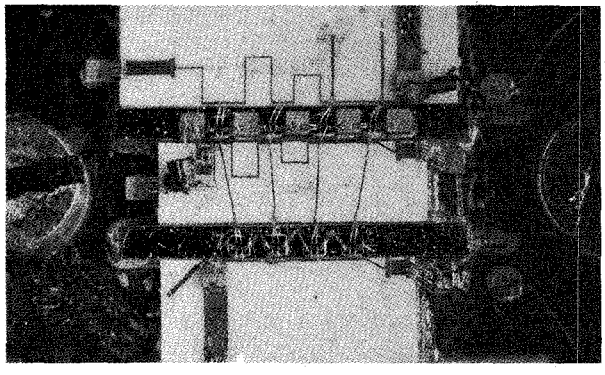


Fig. 9 Photograph of the amplifier module.

Measured gain and noise performance

A very flat gain of approximately 20 dB from 0.5 to 12 GHz and an input and output return loss lower than -10 dB from 0.5 to 16 GHz were measured, as shown in Fig. 10. Measurements were accomplished using the HP-8510B network analyzer with full error correction from 45 MHz to 40 GHz.

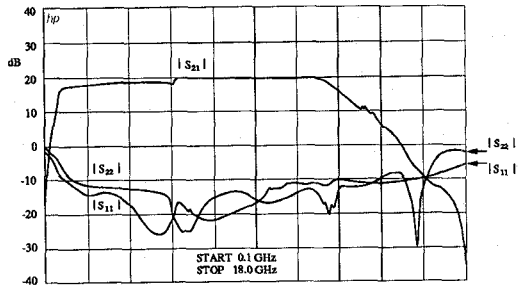


Fig. 10 Measured gain and input-output return loss performance of the amplifier.

Measurements agree rather well with the simulations (Fig. 11) except at the upper end of the band where the measured gain, due to the hybrid realization, starts to fall around 12 GHz.

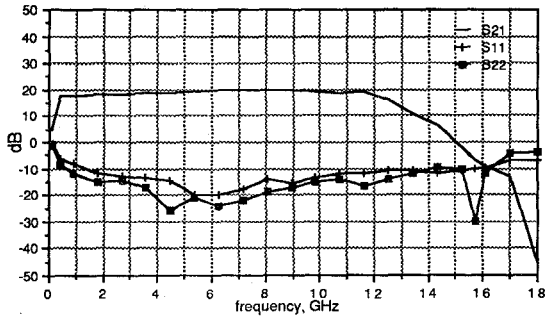


Fig. 11 Computed performance characteristics of the amplifier module.

The amplifier noise figure was measured using the HP 346C noise measurement system and the cascade probe. The curve in Fig. 12 shows approximately 5 dB noise figure from 2 to 11 GHz when the matrix amplifier is biased for maximum gain.

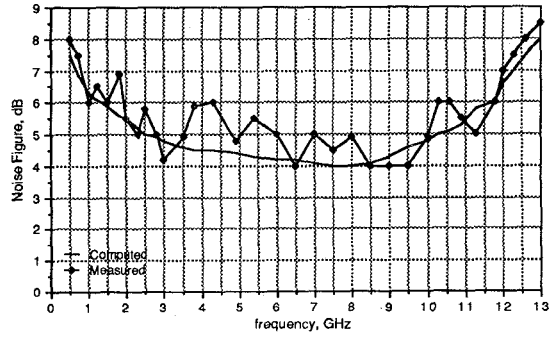


Fig. 12 Computed and experimental noise performance.

Noise figure exceeds 5 dB and is closer to 8 dB near the edges of the bandpass. A good agreement with the theory developed in a previous work [5] has been obtained.

Comparison with an usual distributed amplifier could be meaningful if the same FETs were used in the two cases. However we know from [4] that in this case matrix amplifier gives always better noise performances.

Conclusions

A hybrid 2x4 matrix amplifier using commercial available FET as active devices has been developed: it shows a 20 dB gain in the range 0.5 to 12 GHz with approximately 5 dB of noise figure in the range 2 to 11 GHz. The module has been optimized for applications at a frequency of few hundred MHz (unusual in distributed amplifiers) to several GHz and the experimental results proved the possibility of using the module in measurement instrumentation and in general for wide-band low noise applications as in high bit-rate optical links.

Acknowledgements

The authors would like to acknowledge the support given by ELETTRONICA S.p.A. (Italy), G. Pinto and A. Scatamacchia, in the technical design and assembling of the module.

References

[1] K.B. Niclas and R. R. Pereira, "The Matrix Amplifier: a High-Gain Module for Multioctave Frequency Bands," *IEEE Trans. on Microwave Theory Tech.*, vol. MTT-35, pp. 296-306, Mar. 1987.

[2] S. L. G. Chu, Y. Tajima, J. B. Cole, A. Platzker, M. J. Schindler, "A Novel 4-18 GHz Monolithic Matrix Distributed Amplifier," in *1989 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 291-295, Jun. 1989.

[3] A. P. Chang, K. B.Niclas, B. D. Cantos, W. A. Strifler, "Monolithic 2-18 GHz Matrix Amplifiers," *IEEE Trans. on Microwave Theory Tech.*, vol. MTT-37, pp. 2159-2162, Dec. 1989.

[4] K. B. Niclas, "Noise in Two-Tier Matrix Amplifiers," *IEEE Trans. on Microwave Theory Tech.*, vol. MTT-36, pp. 11-20, Jan. 1988.

[5] S. D'Agostino, G. D'Inzeo, G.Lambertucci, P. Marietti, and G. Panariello, "A Novel Application in Matrix Distributed Amplifier: The Forward-Feed," *Microwave and Optical Tech. Letters*, vol. 3, pp. 354-356, Oct. 1990.

[6] K. B. Niclas, R. D. Remba, R. R. Pereira, B. D. Cantos, "The Declining Drain Lengths Circuits: A Computer Derived Design Concept Applied to a 2-26.5 GHz Distributed Amplifier," *IEEE Trans. on Microwave Theory and Tech.*, vol. MTT-34, pp. 427-435, Apr. 1986.

[7] S. D'Agostino, G. D'Inzeo, P. Marietti, G. Panariello, "A Method for Computing the Noise Figure in Matrix Distributed Amplifier," in *1990 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 351-354, May 1990.